IN THE CLAIMS:

Please cancel claims 1 and 3 in their entirety without prejudice nor disclaimer of the subject matter set forth therein.

1. (Canceled)

2. (Original) An arithmetic circuit comprising:

a first selector to which one input data and a fixed data are inputted wherein these data are selectively outputted in response to a control signal;

a second selector to which another input data and an output data of a register are inputted wherein these data are selectively outputted in response to the control signal;

an inverter circuit for receiving the control signal and outputting an inverted signal thereof;

an adder for receiving an output signal of the first selector and an output signal of the second selector at its addition input terminals, and an output signal of the inverter circuit at its carry input terminal to execute an addition of the output signals of the first and second selectors and the output signal of the inverter circuit; and

a register for receiving an output signal of the adder to hold the output signal in synchronization with a clock signal.

3. (Canceled)